**The paragraph beginning on page 8, line 27 is amended as follows:**

When pins 122-0 and 122-1 reach opposite states of Vcc and Vss, they are allowed to float. Pins 122-0 and 122-1 start to leak toward Vcc/2. At a second predetermined time, tester 110 samples the state each of the pins using Boundary Scan. In one embodiment, sampling the state of each of the pins 122-0 and 122-1 includes measuring a voltage value of each of the pins 122-0 and 122-1. Based on the states or the measured voltage values of pins 122-0 and 122-1, the quality or pass/fail result of pins 122-0 122-1 are determined. Pin to Pin leakage test is further understood [further] with a description of Figure 5.

## IN THE CLAIMS

Please add the following new claims. The new claims are readable on the elected species.

31. (New) A system comprising:
an integrated circuit (IC) including a plurality of terminals; and
a tester connected to the IC to drive a selected terminal among the plurality of terminals to a state at a first time and to determine a state of the selected terminal at a second time different from the first time.

32. (New) The system of claim 31, wherein the tester is configured to apply a supply voltage to the selected terminal at the first time.

33. (New) The system of claim 32, wherein the tester is configured to measure a voltage of the selected terminal at the second time.

34. (New) The system of claim 33, wherein the IC is a Boundary Scan compliant IC.

35. (New) The system of claim 31, wherein the plurality of terminals include a plurality of Boundary Scan terminals, wherein the tester connects to the IC through the Boundary Scan terminals.